

FPDP II - A Data Path to the Future

The successful standardization of FPDP is due, in large part, to the fact that some 30 individual companies have adopted it as an industry standard. As data transfer rate requirements increase, the unprecedented 160 MBytes/second sustained rate of the FPDP is rapidly proving to be inadequate for a number of applications. Therefore, ICS proposes the introduction of FPDP II.

Because the standardization process for FPDP was only finalized this year, ICS feels that any enhancements made to the standard, at this point, should have as little impact as possible on the investment made by the companies that have already adopted FPDP. FPDP II builds on the strengths of FPDP, but more than doubles the bandwidth, from 160 MB/s to 400 MB/s. An attractive feature of FPDP II is that it is backwards compatible with FPDP, reducing the engineering design effort necessary to adopt the new functionality, while allowing legacy designs to continue to work with new products.

When analyzing FPDP, the uncertainty in propagation delays associated with the clock can be regarded as the weak link in any attempt at speed enhancement. Although some speed enhancements have been made to the clock driver and buffer families used by FPDP, they provide only minor improvements. ICS therefore proposes the introduction of PLL technology to provide clock de-skew, in order to dramatically enhance bus timing. Thanks to powerful new technology now becoming available, devices are now available with the following features:

1. The reference clock is selectable between TTL and PECL
2. The outputs have a number of skew options.

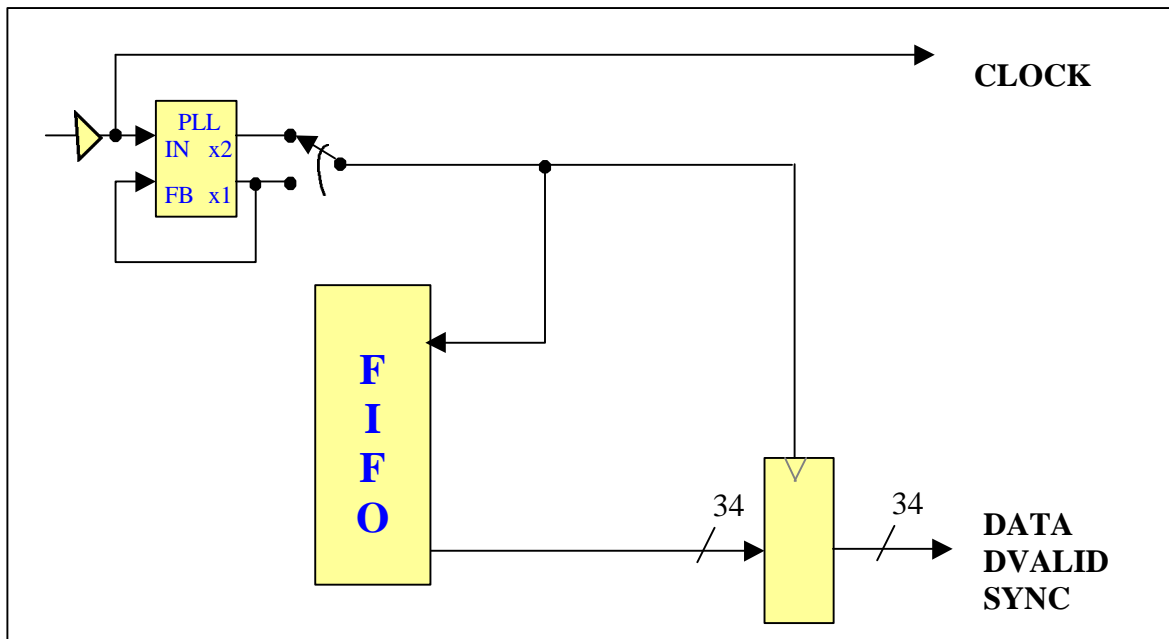


Figure 1 - The Transmit Side of an FPDP II Interface

The same high drive and PECL clock are used to supply the cable clock as for the original FPDP, but for FPDP II, a PLL is used to provide clocks to the output buffers, thus allowing the bus clock frequency to be doubled. Not only does this provide the ability to control the skew of the clock, with respect to the data, but it also introduces the ability to double the frequency of the data clock (referred to as double-edged clocking). This technique greatly improves control of the timing on the bus to the point that, not only can the bus bandwidth be doubled, we believe, but the bus clock itself can be increased from 40 to 50 MHz. This provides an unmatched bandwidth of 400 MB/s (3.2 Gbit/s).

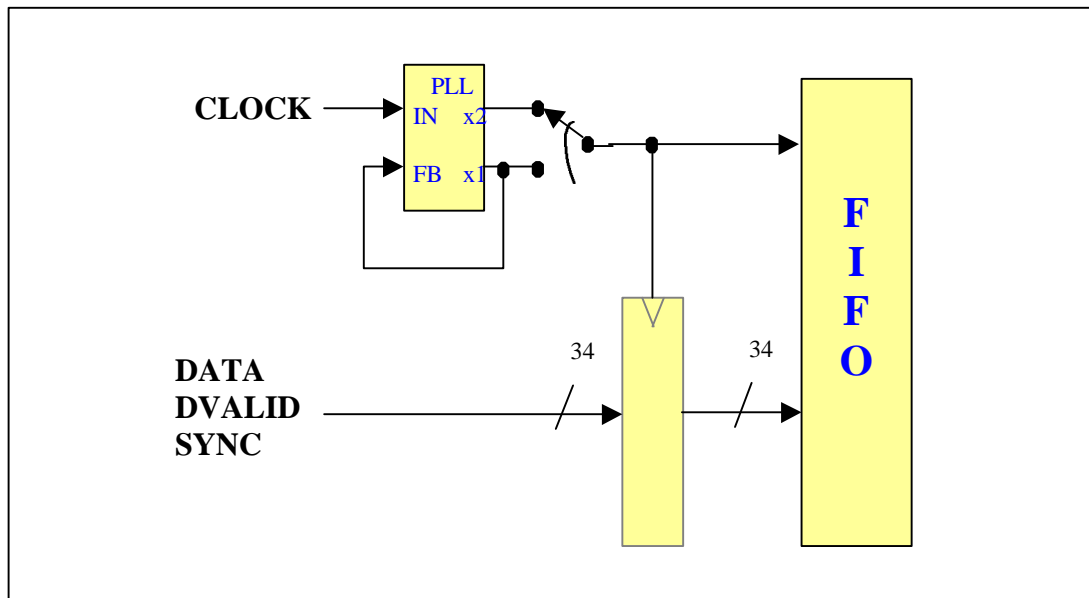


Figure 2 - The Receive Side of an FPDP II Interface

The same advantages can be achieved at the receive interface by de-skewing the incoming clock using a PLL. The required data setup and hold times are improved so that they approach that of the input buffers themselves (2.0 ns and 1.5 ns respectively). Note that this is achieved without any 'real' increase in the bandwidth of the cable itself.

Thus, with relatively little modification to the original FPDP circuitry, an enhancement from 160 MB/s to 400 MB/s can be achieved. Furthermore, the implementation that ICS proposes provides an autodetect feature that switches between the single and double-edged clock by assigning a dedicated pin on the cable. This will provide true backward compatibility. A custom, single chip implementation of the FPDP II interface is under consideration, which ICS would make available to partners interested in adopting FPDP II. ICS looks forward to working with its partners in the development and implementation of FPDP II - A Data Path to the Future!